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Comparative analysis of CMOS and GDI techniques for a 4 bit Multiplier

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Abstract: *VLSI technology has developed over the year's enhancing the performance of chips in terms of two basic constraints viz., delay and power. This paper basically focuses on the implementation of the technique on combinational logic circuits and experimental delay results have been produced. A 4*4 array multiplier can be designed using logical circuits such as AND gate, EXOR gate, Full adder and Half adder .The multiplier is designed using Gate Diffusion Input (GDI) technique. Multiplier is implemented in digital schematic tool. The Layout of the multiplier is obtained and power is calculated in microwind tool along with input and output analysis. This paper shows the comparative study of 4*4 array multiplier using GDI and CMOS technique. The comparative study between GDI and CMOS technique shows GDI is the better one in terms of delay and area.*

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I. Introduction

The most commonly used circuit in the digital devices is Multiplier. To achieve high data throughput most high performance processors rely hardware multiplication. Depending Upon the application in which they are used, there are various types of multipliers available. GDI(Gate
Diffusion Input) a new technique of low power digital combination circuit. The GDI cell is
similar to a CMOS inverter structure. Basic GDI cell consist of three input terminals. They are
1) G-common inputs to the gate of NMOS&PMOS
2) N- input to the source/drain of NMOS
3) P- input to the source/drain of PMOS
Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter

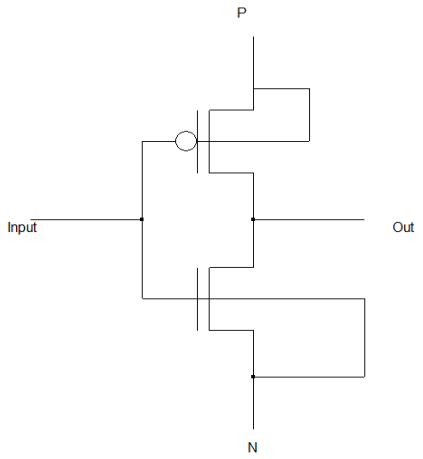

Figure 1: Circuit Diagram of GDI Cell

II. 4 * 4 Array Multiplier using GDI

A 4*4 Conventional array multiplier is known for its regular structure. The Circuit is based on addition and shift algorithm. The partial product is obtained by the multiplication of multiplicand with one bit of multiplier. These partial products are shifted according to their bit orders and then added. The operation of addition is performed by carry propagate adder. For an N bit multiplier, the number of adders required is N-1.

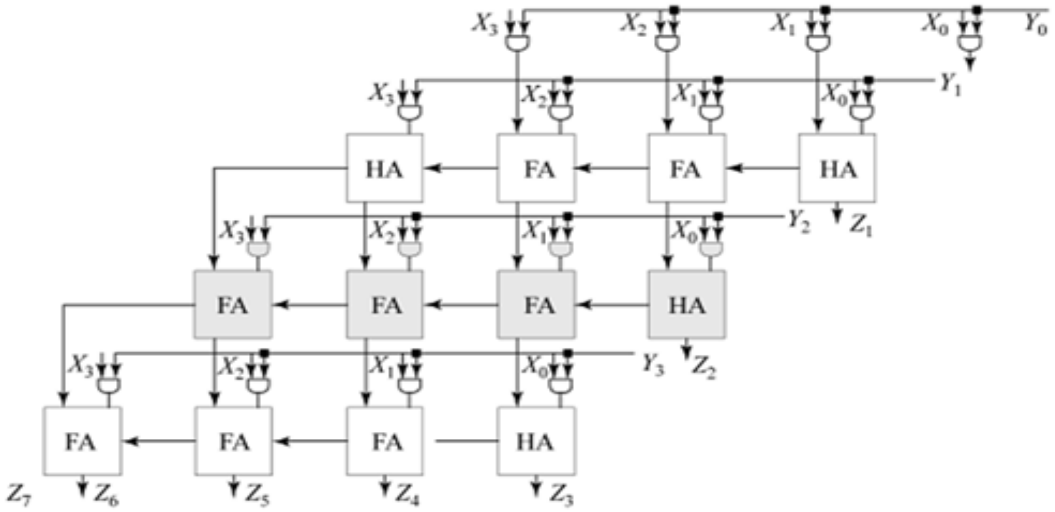

Figure 2: Block diagram of 4*4 Array Multiplier

			x	A3 B3	A2 B2	A1 B1	A0 B0	Inputs
			C	B0 x A3	B0 x A2	B0 x A1	B0 x A0	
		+	B1 x A3	B1 x A2	B1 x A1	B1 x A0		
		C	sum	sum	sum	sum		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			Internal Signals
	C	sum	sum	sum	sum			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	sum	sum	sum	sum				
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Outputs

All the partial product rows of the multiplier are as same as that of the conventional adder. For Example, the fourth carry is given as input to the fifth column instead of zero. The carry of fifth column is forwarded as input to sixth column and so on. The carry of the seventh column of the adder is not neglected. It is considered as Most Significant Bit (MSB).

4*4 Array Multiplier has been implemented using GDI and CMOS technique. The Schematic for the multiplier is given below

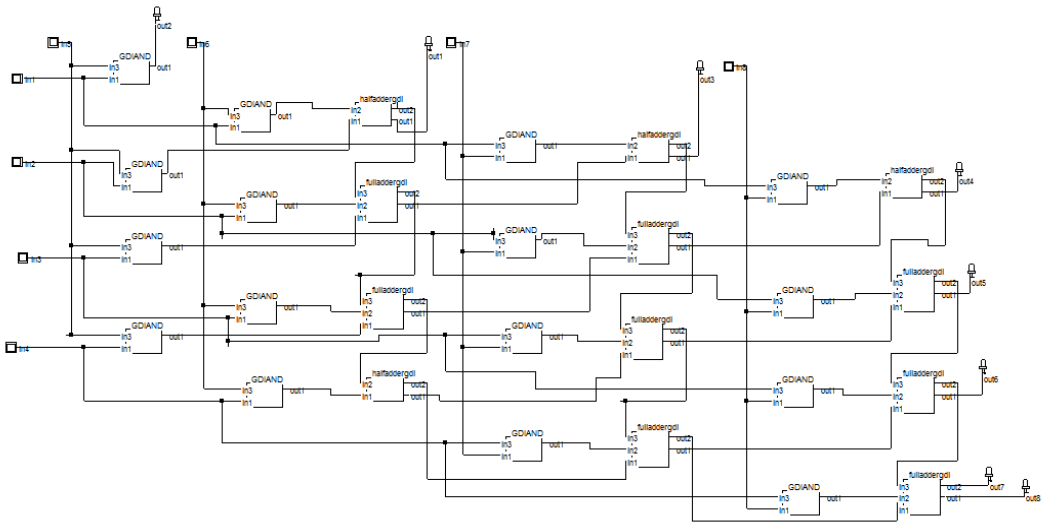

Figure 3: 4*4 array multiplier using GDI cell

III. Implementation and Results

The multiplier is implemented using Digital Schematic and Export Microwind. The tool Digital schematic is used for logic design. Based on primitives, a hierarchical circuit can be built and stimulated. The tool provides delay and power consumption calculation Microwind tool is used for designing and stimulating circuits at layout level. The schematics and Implementation results are given below

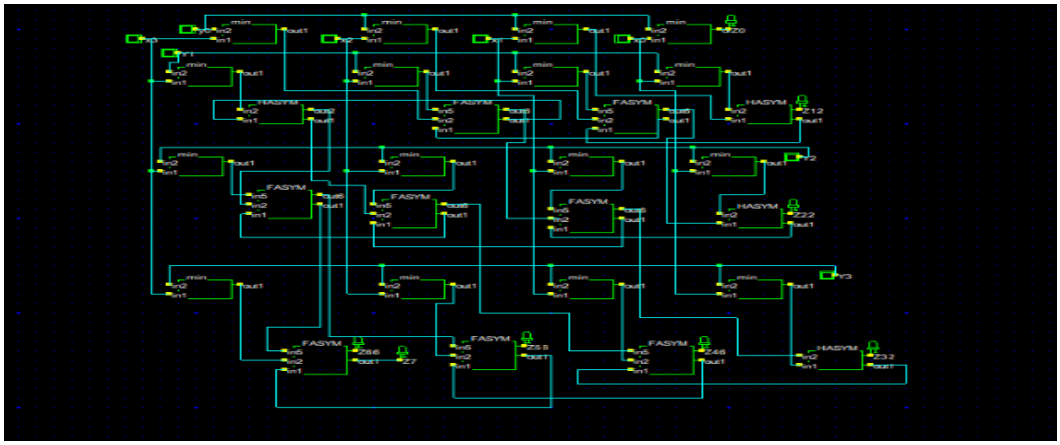

Figure 4: Schematic of CMOS 4*4 Array Multiplier using Digital Schematic tool

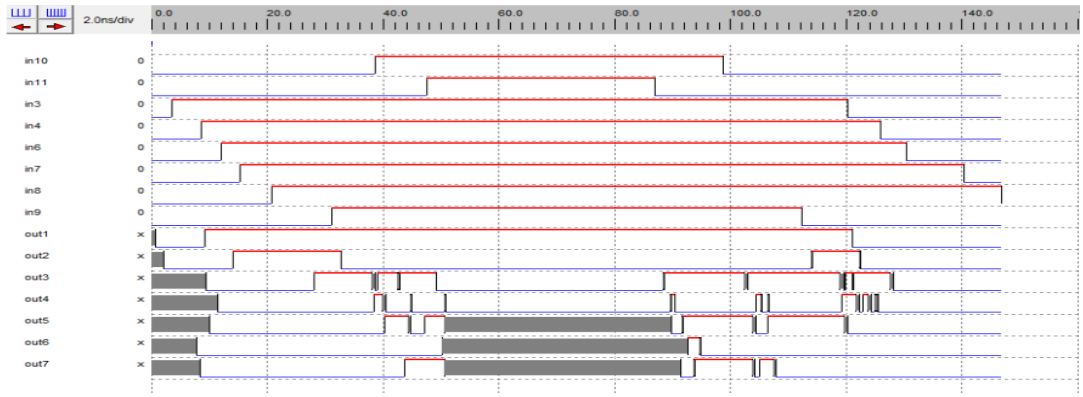

Figure 5: Circuit level Simulation Result of 4*4 Array Multiplier using CMOS in Digital Schematic tool

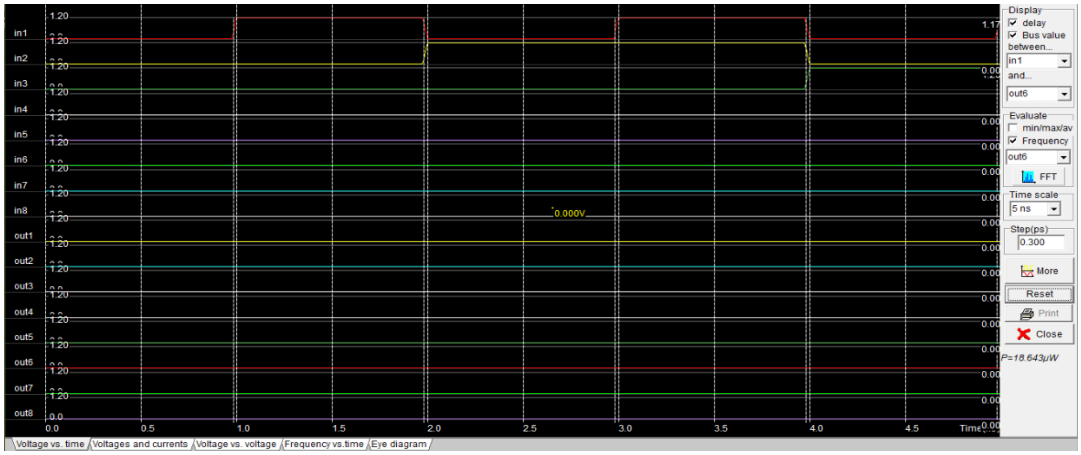

Figure 6: layout Level Simulation result of 4*4 Array Multiplier using CMOS in microwind Tool

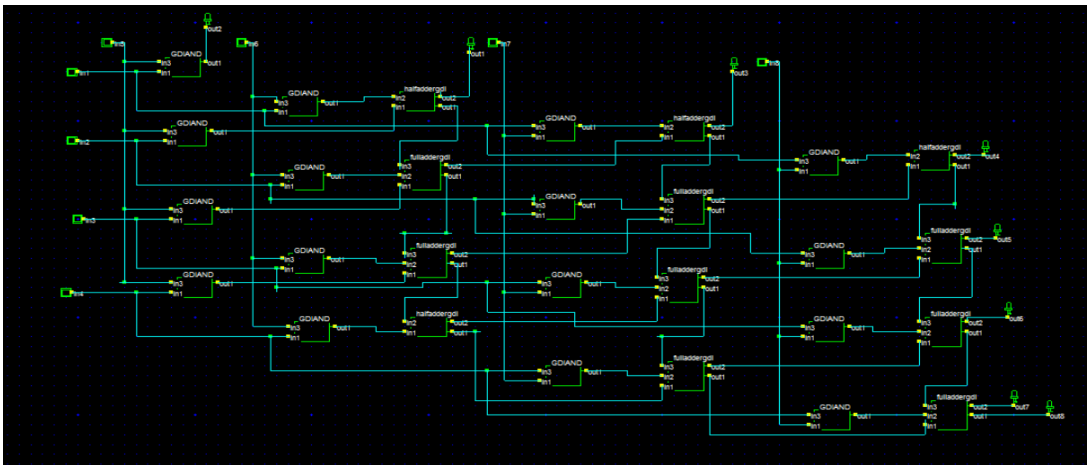

Figure 7: Schematic of 4*4 GDI Array Multiplier using Digital Schematic tool

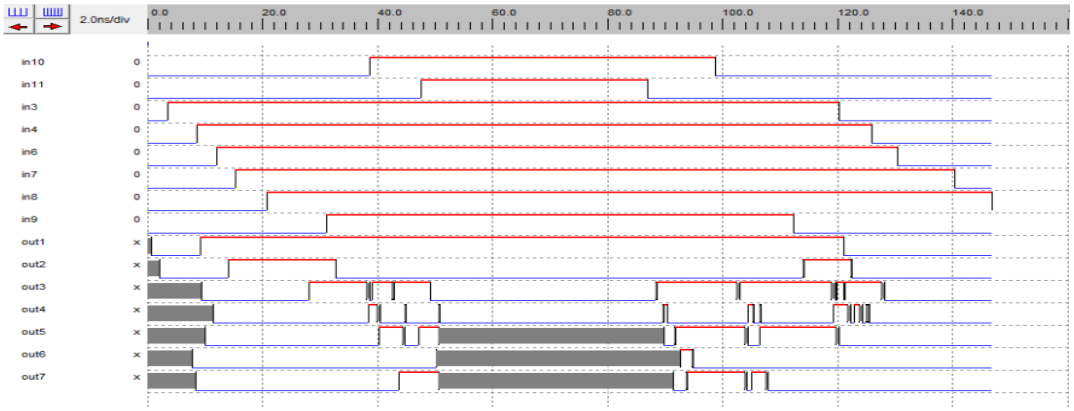

Figure 8: Circuit level Simulation Result 4*4 Array Multiplier using GDI in Digital Schematic tool

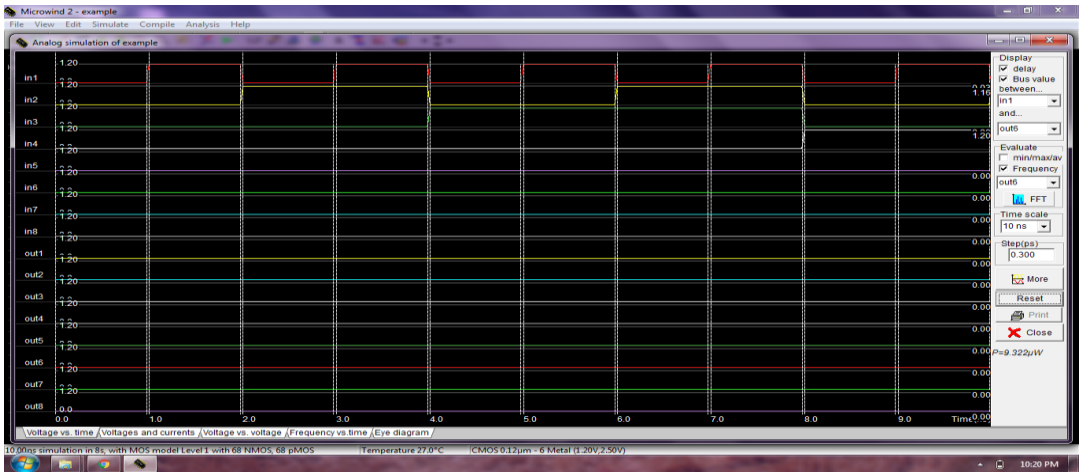

Figure 9: layout Level Simulation result of 4*4 Array Multiplier using GDI in microwind tool

IV. Conclusion

A 4*4 Array multiplier was designed using GDI and CMOS. Numerous logic gates and high-level digital circuits are implemented in various methods and process technologies, and their simulation results are discussed. Comparisons with existing CMOS was carried out, showing an up to 50% reduction of power in GDI over CMOS and significant improvements in performance, as well as decreased number of transistors and area in most simulated GDI circuits over CMOS .In Future perspective higher order multiplier can be implemented using same methodology, pipelining of the circuit can be done to increase the throughput. A low swing multiplier can be designed by Modified Gate Input Diffusion technique.

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